Energy Efficient Computing SIG – Thursday 18th July

Background Information

Power consumption is a critical element of today's computing devices:

- Even the smartest smart phone or tablet stops working when the battery runs out of power!
- The predicted limit of the fastest supercomputer is based on the total amount of power consumed rather than compute performance.
- Most of the predicted 50Billion devices in the Internet of Things will not be connected to mains – so cannot send data if they run out of power.

The use of digital devices and systems – big or small, complex or simple - are already essential for the intelligence and automation that supports our daily lives… and they all consume power. In portable devices there is a constant balancing act between graphics, processing and battery life. The large computer systems that are required for data modeling and processing in today's "Big Data" society are also a significant proportion of the electricity consumption of developed economies.

The power consumption of a device can set an upper bound on performance available – hence the need for more power efficient compute platforms.

The Energy Efficient Computing SIG (EEC SIG) was funded by the Technology Strategy Board to provide a focus for innovations in this area of technology. It brings together the communities of ICT KTN and ESP KTN. One particular perceived challenge was that reductions in power consumption in hardware alone were no longer sufficient to achieve the required performance. It was essential to gain a better understanding of the problem and then address the solutions as a systems problem – requiring the combined skills of software, hardware and systems design.

This meeting will present some of the work undertaken in the first year of operation of the SIG and a wide range of presentations that cover current and future work being undertaken in industry and research organisations. It will also cover future support and **funding schemes** from both the Technology Strategy Board and the EU.

Anyone working with compute platforms will find something of interest – see next page for an overview of the sessions. Plus there will be an opportunity to network with other experts from the sector to share knowledge and seek collaborations.

The event is free to attend and will be held at the Ambassadors Bloomsbury Hotel

To Register go to http://eec-year1.eventbrite.co.uk

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Overview of Sessions

The event will open with Jonathan Mitchener, Lead Technologist for Technology Strategy Board, who will cover the Technology Strategy Board funding support for innovation and the focus of the Emerging Technology and ICT strategies.

The next session will a review of the work that has been funded by the EEC SIG. One project was starting work on **Community Mapping** - a study on the organisations within the UK active in EEC. Another very interesting project looked at the "**Energy Cost of an Internet Transaction**" – this is a very critical area as computers represent a significant, and growing, percentage of global power consumption. The third project provided a review of **software tools** that focus on power.

During the last year Technology Strategy Board held a funding completion for innovations in energy efficient computing and two of the winners, **Zenotech** and **Embecosm**, will present a review of their project and the current progress. These may well include demonstrations and the latest news from the GNU tools conference in California.

In the next session **Kerstin Eder** of Bristol University will present on some of the work being funded by the EU and in particular her project: "ENTRA: Whole-Systems Energy Transparency".

The main **EU funding** strategies are still being formulated but a clearer picture is beginning to emerge. The afternoon will start with Panagiotis Tsarchopoulos from EU DG Connect Future & Emerging Technologies who will cover the latest thinking on relevant **Horizon 2020** funding schemes that are anticipated.

Prof Al-Hashimi will cover the new, £5.6M EPSRC funded, **Power-efficient, Reliable, Many-core Embedded systems** (**PRiME**) project. Involving many of the UK's leading experts, from several research organisations, this project will be significant in the development of future EEC systems.

The **Hartree Centre** is located at Daresbury and is jointly funded by STFC and IBM. It recently won over £20M additional funding for work in the area of HPC platforms for systems to support Big Data from the UK Science Budget. Looking at the most energy efficient designs for the HPC platforms of tomorrow.

Tim Whitaker of **Cambridge Consultants** will present on the "real world" implications of power consumption for product design.

Finally there will an open discussion to bring together the themes from the presentations and I will cover an overview of the future programme for the SIG. This is a session where we listen and seek input.

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Programme

10:00 Introduction and Welcome
Nigel Rix, ESP KTN

10:05 The TSB EEC Programme & Competition
Jonathan Mitchener, Technology Strategy Board

10:30 The EEC Community Map Project & Software Tools Project
Phil Williams & Nigel Rix, ESP KTN

11:00 The Energy Cost of an Internet Transaction Project
Kate Craig-Wood, Memset, or Paul Krause, Univ of Surrey

11:30 Refreshments / Networking

11:45 Global Register for Energy-Efficient Numerical Simulation
David Standingford, Zenotech

12:00 MAchine Guided Energy Efficient Compilation (MAGEEC)
Jeremy Bennett, Embecosm

12:30 ENTRA: Whole-Systems Energy Transparency
Kerstin Eder, Bristol University

13:00 Lunch / Networking

14:00 Horizon 2020 perspectives
Panagiotis Tsarchopoulos, Future & Emerging Technologies-DG CONNECT

14:30 Power-efficient, Reliable, Many-core Embedded systems (PRiME)
Prof. Bashir Al-Hashimi, University of Southampton

14:55 The Hartree Centre: Designing tomorrows HPC platforms
Jonathan Follows, STFC

15:20 Refreshments / Networking

15:45 Energy efficient comms for energy efficient computing
Tim Whittacker, Cambridge Consultants

16:10 The EEC SIG Programme & Panel Session/General Discussion
Nigel Rix, ESP KTN

16:30 Networking

17:00 Close

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Special Interest Group
Energy Efficient Computing

Presentation Details

UK Energy Efficient Computing Sector

This study surveys UK company activity and academic research in the field of energy efficient computing across the sectors of HPC, data centres, parallel and multi-core architectures, embedded systems, devices, compilers and software tools.

Software Tools Study

This paper provides an overview of some technologies and features provided by a selection of processor manufacturers and third-party tool vendors to assist embedded and application software developers to write energy-efficient code.

Estimation of the energy cost of Internet mediated transactions

We have undertaken a comprehensive audit of the energy budget of transactions mediated by the Internet. Our analysis yields a figure of 1592 Wh/GB for the energy consumed (embedded plus in use) in transferring data from a regional data center to an end user (based on the average British bandwidth consumption of 23 GBytes per month). This is significantly lower than earlier published estimates, but this difference can be accounted for by efficiency gains over the last seven years.

Our analysis demonstrates that this energy budget is dominated by the figures for the data center and the interface between ISP and consumer/office. It is possible that these efficiency gains are being countered by increased resource consumption. However, these additional Internet mediated activities often replace other activities with significantly higher energy budgets. We illustrate with the case of media streaming that the rebound effect that many have predicted for ICT might not be realized within the broader context of a typical (Western) human's energy footprint.

Global Register for Energy-Efficient Numerical Simulation (GREENS)

Engineering complex products (aircraft, buildings, wind turbines & motor vehicles) makes extensive use of high fidelity computer modeling. This requires power-hungry computer hardware & specialist software. a bewildering array of options is presented to the end user: hardware, software & algorithm selection – with their own measures of "performance" value chain stakeholders would benefit from a standard measure of energy efficiency – so that the devices, systems and software energy use can be measured and characterized.

This will inform user choices, and motivate component improvement with a specific value proposition.

MAchine Guided Energy Efficient Compilation (MAGEEC)

All computer systems depend upon compilers to convert programs into a binary format that computer hardware can execute (known as an executable). This compilation process needs to generate executables that are as efficient as possible. To date, compilers have emphasised speed of the executable.

Building on the UK's existing leadership in this field, this project will create a prototype infrastructure for existing compilers to instead generate executables which minimise the energy used by the computer hardware. This will be the first time anyone has attempted this.

We will then try to improve existing compilers to further reduce the energy consumption of the executables, so delivering cost, environmental and battery life benefits. While the consortium will gain directly in reputation and commercial advantage, the results of this project will be open source and thus freely available, helping the wider UK engineering community to maintain their leadership in this field.

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ENTRA: Whole-Systems Energy Transparency

ENTRA is a 3-year research project funded by the EU 7th Framework Programme Future and Emerging Technologies (FET). The project runs from the 1st October 2012 to the 30th September 2015 and aims to promote "energy-aware" software development using advanced program analysis and modelling of energy consumption in computer systems.

The project will facilitate predictions of energy consumption to be made early in the software design phase, thus enabling the development of greener IT products.

Power-efficient, Reliable, Many-core Embedded systems (PRiME)

PRiME is a £5.6M grant from EPSRC to bring together a number of UK universities. Our vision is to enable the sustainability of many-core scaling by preventing the uncontrolled increase in energy consumption and unreliability through a step change in holistic design methods and cross-layer system optimisation.

PRiME seeks to establish the new science and engineering that is needed to design future high-performance, energy-efficient and reliable embedded systems with many-core processors.

Energy efficient comms for energy efficient computing

To be confirmed

The Hartree Centre: Designing tomorrows HPC platforms

The Hartree Centre is focused on this future and on making it happen.

One potential brake is the failure of software to keep pace with hardware developments. A key objective of the Hartree Centre is to bridge this gap and ensure the availability of code that can run effectively on next generation supercomputers.

Our fundamental goals are to:

- Help organisations unleash the full power, versatility and value of HPC
- Add momentum to the development of high-tech, knowledge-led economies