InAlAs/InGaAs solar cells: moving towards the InP Lattice parameter for multi-junction III-V Photovoltaics

Donagh O’Mahony, III-V Materials and Devices Group, Tyndall National Institute, University College Cork, Ireland
Tyndall: Key Facilities

- Silicon & Compound Semi Fabs
- MOVPE, ALD growth
- Electrical & Reliability Analysis
- Photonics Packaging

www.tyndall.ie
Why move towards the InP lattice parameter?
Simulation: 56.1% efficiency for optimised 3J (x500, AM1.5d) Exceeds conventional (~GaAs parameter) 3cell by >3%

www.tyndall.ie
Alternative Multi-Junction Concept

Leite et al, IEEE (PVSC), 2012
[Caltech/Spectrolab]

Walters et al, IEEE (PVSC), 2011
[NRL/Imperial College]
Leite et al., APL, v98 2011 (h =14.2%)  
Woo et al., PVSC 2011 (h =13.8%)
Key Issues

• **InP substrates**
  - Cost (vs Ge, GaAs)
  - Scalability (6”, 8” feasible with InP???)

• **For maximum Efficiency.....**
  - Need substrate with intermediate parameter
Mathews et al., EU PVSEC, 2013

Efficiency Maximised near I (but not equal to!) InP parameter
Graded Substrate Approach (Tyndall, 2013)

InAlAs solar cell on a GaAs substrate employing a graded In$_x$Ga$_{1-x}$As–InP metamorphic buffer layer

Ian Mathews,1,2,4 Donagh O’Mahony,1 Agnieszka Gecalinska,1 Marina Mangano,1 Emanuele Pelucchi,1 Michael Schmidt,1 Alan P. Morrison,1,3 and Brian Corbett1
1Tyndall National Institute, Lee Maltings, University College Cork, Cork, Ireland
2Department of Electrical and Electronic Engineering, University College Cork, Cork, Ireland

Graded Substrate (Metamorphic Buffer Layer)
Design 1:
• Shallow Base (~500nm)
• Nom. 65% Al FSF
• Planar (lateral) contacting
  • N.U.D. MBL

Figure 5: Current-Voltage (I-V) characteristics of the InAlAs solar cells in the dark ($J_D$, right-hand scale) and under 1-Sun illumination ($J_L$, left-hand scale). The performance of the device grown on the virtual substrate is indicated by the dashed lines.

<table>
<thead>
<tr>
<th></th>
<th>$J_{sc}$</th>
<th>$V_{oc}$</th>
<th>FF</th>
<th>Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>n-type substrate</td>
<td>17.6</td>
<td>0.92</td>
<td>79</td>
<td>12.8</td>
</tr>
<tr>
<td>Virtual substrate</td>
<td>12.31</td>
<td>0.72</td>
<td>75</td>
<td>6.6</td>
</tr>
</tbody>
</table>
Design 1:
- $10^5$ increase in leakage for MBL
- IV indicates shunting
- x2 decrease in EQE

InP substrate

MBL (GaAs) substrate
InAlAs 1J: Optimisation on InP

**Bandgap**
- GaAs (300 K) = 1.41 eV
- In$_{0.52}$Al$_{0.48}$As (300 K) = 1.45 eV

**Bandgap voltage offset**
- $E_g - V_{oc} \approx 400$ mV for ‘good cell’ (King et al.)
- GaAs: 388 mV
- InAlAs: 466 mV – good but can be improved, how?

<table>
<thead>
<tr>
<th>Cell</th>
<th>Efficiency (%)</th>
<th>$V_{oc}$ (mV)</th>
<th>$J_{sc}$ (mA/cm$^2$)</th>
<th>FF (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaAs</td>
<td>22.44</td>
<td>1022</td>
<td>26.62</td>
<td>82.5</td>
</tr>
<tr>
<td>InAlAs</td>
<td>13.8</td>
<td>984</td>
<td>17.6</td>
<td>79.6</td>
</tr>
</tbody>
</table>

Limited to ~14%?

Close to SOA

Highest $V_{oc}$ measured for an InAlAs cell to date
Bottom cell development: InGaAs

<table>
<thead>
<tr>
<th>nm</th>
<th>Layer</th>
<th>cm$^{-3}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>200</td>
<td>p-In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>1e19</td>
</tr>
<tr>
<td>140</td>
<td>SiN (n~1.95)</td>
<td>ARC</td>
</tr>
<tr>
<td>100</td>
<td>p-InP</td>
<td>2e18</td>
</tr>
<tr>
<td>100</td>
<td>p-In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>2e18</td>
</tr>
<tr>
<td>3000</td>
<td>n-In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>3e17</td>
</tr>
<tr>
<td>500</td>
<td>n-InP</td>
<td>1e19</td>
</tr>
<tr>
<td></td>
<td>n-InP</td>
<td>1e18</td>
</tr>
</tbody>
</table>

InP substrate
InGaAs 1J: InP vs GaAs (MBL) substrates

Both $V_{oc}$ and $J_{sc}$ reduced for MBL(GaAs) vs InP substrate

<table>
<thead>
<tr>
<th>Sub.</th>
<th>$V_{oc}$</th>
<th>$J_{sc}$</th>
<th>FF</th>
<th>H</th>
</tr>
</thead>
<tbody>
<tr>
<td>InP</td>
<td>357</td>
<td>38.2</td>
<td>69</td>
<td>9.3</td>
</tr>
<tr>
<td>GaAs</td>
<td>272</td>
<td>28.6</td>
<td>56.5</td>
<td>4.4</td>
</tr>
</tbody>
</table>
Summary

- **Progress to date**
  - Cells with lattice parameter near InP demonstrated
  - Graded substrate (MBL) developed
  - InAlAs on InP substrate with near SOA efficiencies

- **Ongoing development:**
  - Is InAlAs 1J efficiency limited ~14%?
  - Suitable FSF/window needed ($\text{In}_{1-x}\text{Al}_x\text{As}$ with $x>60$%)?
  - Heterostructure effects (InAlAs/InP type II interface?)
  - MBL substrate: Ultimately limited by defects?
• Enterprise Ireland (MODCON-PV project)
• ENIAC JU (ERG project)
• SFI TIDA (ASICS project)

Ian Mathews¹, ², ³, Donagh O’Mahony¹, Agnieszka Gocalinska¹, Emanuele Pelucchi¹, Kevin Thomas¹, Alan P. Morrison¹, ² and Brian Corbett*, ¹

¹Tyndall National Institute, Lee Maltings, University College Cork, Ireland
²Dept. of Electrical and Electronic Engineering, University College Cork, Ireland
³Efficient Energy Transfer (ηET) Dept., Bell Labs Ireland, Alcatel-Lucent, Dublin, Ireland